

REMARKS

Informalities

In the Office Action mailed on May 30, 2007, the Examiner objected to the drawings because they failed to show a demodulating circuit as described in the specification. The Examiner is requiring corrected drawing sheets to illustrate the demodulating circuit.

Applicants wish to point out that the demodulating circuit is a logic element **72** on FIG. 1, and as such a demodulating circuit is depicted in the drawings for the instant application. In the specification, in the paragraph starting on page 9 at line 27, Applicants discuss the types of logic circuits that could be used for the demodulating circuit **72** at the “receive end” of the system of the present invention. In this paragraph, Applicants noted that the logic element **72** could comprise an exclusive-OR (XOR) gate or an exclusive-NOR (XNOR) gate in the present invention, and also discussed an alternative circuit in which the logic element **72** could comprise a differential receiver.

The preceding paragraph of the instant application (i.e., the paragraph starting on page 9 at line 17) discusses the fact that the signals are demodulated at the “far end” of the cable run, in which the transmission end has two DATA_OUT signals referred to as TX1 and TX2, and these signals are referred to on FIG. 1 by the reference numeral **60**. On the receive end, the signals are referred to as RC1 and RC2, and are referred to as a group by the reference numeral **70**, and these receive signals RC1 and RC2 are directed as inputs to the logic element **72**. Therefore, the logic element **72** is the “receive end” of the modulation-demodulation circuit pair, and the output of the logic element **72** is referred to as the signal **74**.

Applicants have submitted a substitute set of drawings, in which new drawings for FIG. 8 and FIG. 9 are being entered with this Amendment. FIG. 8 illustrates the logic element **72** as being an exclusive-OR gate, while FIG. 9 illustrates the element **72** as an exclusive-NOR gate. These are examples of the types of receiver circuits or “demodulating circuits” that could be used in the present invention, and they are the simpler types of circuits which are described in the paragraphs noted above. Therefore, no new matter is involved by entering these new drawings for FIG. 8 and FIG. 9.

Changes to Drawings

A set of substitute drawings is enclosed herewith. New FIGS. 8 and 9 are being added to

show examples of a “demodulation circuit” 72. In FIG. 8 the demodulation circuit comprises an Exclusive-OR (XOR) gate, which is discussed in the written description on page 9, lines 29-30. In FIG. 9 the demodulation circuit comprises an Exclusive-NOR (XNOR) gate, which is discussed in the written description on page 9, lines 29-30. The symbols depicted on FIGS. 8 and 9 are industry standard symbols for such logic gates.

As noted above, FIGS. 8 and 9 are added as new drawings with this Amendment. Substitute drawings for FIGS. 1-7 are also enclosed to show the correct number of sheets on the drawing pages. Since the example XOR and XNOR gates are described in the specification (as noted above), Applicants believe that no new subject matter is involved in FIGS. 8 or 9.

Claim Objections

The Examiner objected to claims 2, 11, and 21 because of fairly minor incidents concerning antecedent basis wording. Applicants have amended these claims along the lines suggested by the Examiner, and appreciate the Examiner’s helpful suggestions.

Claim Rejections; Antecedent Basis

Claims 9, 19, and 21 were rejected as lacking antecedent basis. Applicants have amended these claims to correct the incidents described in the Office Action.

In addition to the antecedent basis incidents noted by the Examiner in the Office Action, Applicants have also amended claims 21 and 22 to correct the phrase “edge transitions” to instead read --transitions--.

The above amendments to the claims are being made solely for the purpose of overcoming § 112 objections by the Examiner; those amendments are not for a reason related to patentability in view of prior art.

"Objected To" Claims

In the above-identified Office Action, the Examiner stated that claims 2-6, 11-15, and 20-22 comprised allowable subject matter if they would be rewritten in independent form. Claims 2, 6, 11, 15, and 20 have been placed into independent form by this Amendment document, and they include the subject matter of their respective base claims (i.e., claims 1, 10, and 20, as required).

Prior Art Rejections

In the above-identified Office Action, the Examiner rejected certain claims as being anticipated by Asano (US 5,793,988). This rejection included claims 1, 7, 9, 10, and 16. Of these rejected claims, claims 1 and 10 are independent. Moreover, the Examiner rejected certain claims as being obvious in view of the combination of Asano and Lo (US 6,026,141), and in this category claim 17 is the independent claim.

The Asano patent is the primary reference noted in the above-identified Office Action. In general, the Asano patent takes a stream of data (i.e., multiple bytes of serial digital data) and randomizes the data at a signal modulator **100**, then runs that modulated data through an interface cable **30**, and at a receiving end demodulates the modulated data at a signal demodulator **200**. In a primary mode of the Asano invention, there are counters **110** and **210** that increment or decrement the initial value of the data, depending on whether the circuits are employed as data modulators or data demodulators. The modulator can increment a data byte, and at the receiving end the demodulator can decrement that same data byte, thereby restoring the data to its original value.

There is nothing in Asano that teaches or suggests that the frequencies of the modulated data have any relation to the original frequencies of the original data. Instead, Asano is attempting to “randomize” the data, as indicated at a number of places in the Asano patent, including in the Summary (see column 3, lines 10-15), and in the Detailed Description of the Preferred Embodiment (see column 7, lines 5-8).

In the instant application, claims 1, 10, and 17 have each been amended to describe in greater detail the effect of the data modulation by the circuits or methods of the present invention. In claim 1, a modulating circuit repetitively modulates the input data signal according to a predetermined modulation cycle, which comprises at least one modulating pattern set. Claim 1 has been amended to state that the “at least one modulating pattern set comprises a set of sideband frequencies that exhibit distinct patterns of electromagnetic energy.” Claim 10 has a similar element added by this Amendment, except in claim 10 the modulation cycle comprises “at least two modulating pattern sets.” For claim 10, each of the at least two modulating pattern sets comprises a set of sideband frequencies that exhibit distinct patterns of electromagnetic energy.

Claim 17 is an apparatus claim, which includes a modulating circuit that manipulates the data input signal in a manner that generates concentrations of electromagnetic energy emissions near a frequency of the data input signal. Claim 17 has been amended to state that the

“concentrations of electromagnetic energy emissions of said first output data signal comprise a set of sideband frequencies that exhibit distinct patterns of electromagnetic energy.”

By using the concentrations of electromagnetic energy emissions to generate a set of sideband frequencies about the fundamental frequency and certain harmonic frequencies of the originating data signals, the present invention has better control over the overall energy emissions of the data transmitting system, as compared to the system disclosed in the Asano patent. Support for the amendments to these claims is found in the Detailed Description of the Invention on page 7, lines 8-14, and also on page 7, lines 15-27 (with further information about the sideband frequencies), and also on FIG. 7, which graphically shows the effect of the sidebands. A discussion of FIG. 7 is found in the instant application on page 23, line 31, through page 24, line 18.

In view of the amendments to the independent claims 1, 10, and 17, Applicants respectfully submit that these claims are not rendered obvious or anticipated by the cited prior art references. The dependent claims that have also been rejected should be in condition for allowance in view of the amendments to the independent claims discussed above.

New Claims

Applicants have added two new dependent claims, numbers 26 and 27. These claims depend from claim 13, which already consists of allowable subject matter. The subject matter of claims 26 and 27 is discussed in the DETAILED DESCRIPTION in multiple locations, and more specifically on page 22, lines 7-10.

Conclusion

Applicants have amended the independent claims and have provided reasoning arguing for the patentability of those amended independent claims. Applicants have converted certain dependent claims that were “objected to” into independent form, and those claims should be in condition for allowance, along with their respective dependent claims. Applicants have corrected certain claims with regard to antecedent basis objections or rejections, and those rejections should now be obviated. Finally, Applicants have submitted a substitute set of drawings that include a new FIG. 8 and FIG. 9 to show examples of a demodulating circuit, as required by the Examiner.

Payment of Additional Fees

Applicants are transmitting a fee payment form to pay for additional independent claims, two new "total" claims, and also to pay for a two-month extension of time. The Director of Patents and Trademarks is hereby authorized to charge any underpayment or credit any overpayment of fees incurred due to this amendment to Deposit Account No. 20-0095.

Applicants respectfully request the Examiner to favorably reconsider and allow all of the pending claims.

Respectfully submitted,
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